CLAIMS

What is claimed is:

1. A method of operating an amplifier, which amplifier has an load line,

to emulate the property of a class AB amplifier where increasing amplifier input current raises the d.c. bias of the amplifier and increases amplifier output current,

nonetheless that the amplifier will never enter class AB operation and will always operate in class A,

the method of operating an amplifier always in class A nonetheless to producing more output current from more input current comprising:

monitoring the amplified output of the class A amplifier; and, in response to detecting an increase in the amplifier output,

dynamically biasing the load line of the amplifier to a higher d.c. bias point, causing the amplifier to consume more power and to produce a still larger amplified output signal, nonetheless to maintaining operation of the amplifier always in class A.

2. The class A amplifier operating method according to claim 1 used on a class A amplifier serving as an initial low noise radio signal amplifier in a wireless communication system;

wherein an increase in amplifier output signal is indicative of a presence of a strong jammer component in the amplifier input signal, so that moving the load line of the amplifier will cause the amplifier to draw more current beneficially decreasing a noise figure while increasing gain of the amplifier, and causing the amplifier to reach a new steady state with higher power and improved linearity.

wherein when no increase in amplifier output signal is detected, indicative that no strong jammer component is present within the amplifier input signal, then neither the d.c. bias, nor the load line, will be raised, and the amplifier will operate

quiescently, conserving power.

3. An amplifier comprising:

at least one Field Effect Transistor (FET) receiving at its gate an input signal from an external source and amplifying this input signal in accordance with its drain-source bias voltage V_{DS} to produce at its drain an amplified output signal;

a power detector circuit monitoring the amplified output signal to produce a detected-power voltage signal V_{DD}; and

a dynamic bias control circuit comparing the detected-power signal V_{DD} to the drain-source bias voltage V_{DS} to vary a gate-to-source voltage bias V_{GS} of the input signal, actively moving a load line of the FET so as to cause the FET to consume more power when the amplified output signal is large;

wherein when the amplified output signal is large because of a presence of a strong jammer component of the input signal, then the moved load line of the at least one FET will cause the FET to draw more current decreasing noise figure while increasing gain, and will cause the amplifier of which the at least one FET forms a part to reach a new steady state with higher power and improved linearity;

wherein, however, when no strong jammer component of the input signal is present, and when the amplified output signal is correspondingly not large, then the FET, and the amplifier of which it forms a part, will conserve power;

wherein a self-adjusting bias of the at least one FET results in improved power consumption and improved dynamic range in an environment where exists occasional strong jammer signals.

4. The amplifier according to claim 3 wherein the at least one Field Effect Transistor (FET) comprises:

two cascaded FETs.

5. The amplifier according to claim 4 wherein the each of the two

cascaded FETs comprises:

a GaS FET.

6. The amplifier according to claim 4 wherein a first, input, one of the two cascaded FETs comprises:

a low-noise PHEMT;

and wherein a second, output, one of the two cascaded FETs comprises:

a hetero-junction FET.

7. The amplifier according to claim 3 wherein the dynamic bias control circuit comprises:

two operational amplifiers each varying a gate-to-source voltage bias V_{GS} of an associated FET.

8. The amplifier according to claim 3 wherein the power detector circuit comprises:

a resistor R; and

a first diode D_1 series connected to form a diode-limited resistive divider.

9. The amplifier according to claim 8 wherein the diode-limited resistive divider and first diode D_1 are both temperature compensated by a second diode D_2.

10. The amplifier according to claim 3 wherein the power detector circuit is temperature compensated.

11. The amplifier according to claim 3 operational in S band.

12. A low-noise amplifier (LNA) improved for having an elevated third-order input intercept point (IP3) and reduced noise figure during jamming, the LNA comprising:

at least one active device amplifying in accordance with a

bias signal an input signal received from an external source so as to produce an amplified output signal;

a power detector monitoring the amplified output signal to produce a detected-power signal; and

a dynamic bias control circuit responsive to any difference between the detected power signal and the bias signal to increase the bias signal, actively moving a load line of the at least one active device so as to cause this device to consume more power when the amplified output signal is large;

wherein when the amplified output signal is large because of a presence of jamming then the moved load line of the at least one active device will cause the active device to draw more current, decreasing noise figure while increasing gain, and will cause the amplifier of which the at least one active device forms a part to reach a new steady state with higher power and improved linearity.

13. The LNA according to claim 12 further improved for conserving power, the power detector and the dynamic bias control circuit and the at least one active device functioning so that when no jamming is present then, at nominal small-signal conditions, the at least one active device is biased to consume less power, conserving power in the amplifier of which it forms a part.

14. A method of low-noise amplification improved for

(i) conserving power during nominal small-signal conditions but also for

(ii) increasing its gain and reducing its noise figure during jamming, making less likely any loss of data, while

(iii) increasing its linearity, particularly as measured by a second-order intercept point IP2 and a third-order intercept point IP3, during jamming, the increased linearity reducing any signal distortion caused by jamming and again making less likely any loss of data,

the method comprising:

amplifying in at least one active device and in accordance with a bias signal an input signal received from an external source so as to produce an amplified output signal;

monitoring in a power detector the amplified output signal to produce a detected-power signal; and

adjusting, in a dynamic bias control circuit responsively to any difference between the detected power signal and the bias signal, the bias signal of the at least one active device so as to actively move a load line of this at least one active device and cause this at least one active device to consume more power when the amplified output signal is large;

wherein when the amplified output signal is large because of a presence of jamming then the moved load line of the at least one active device will cause the active device to draw more current, decreasing noise figure while increasing gain and increasing linearity, and will cause the amplifying to reach a new steady state with higher power and improved linearity;

wherein when no jamming is present then, at nominal small-signal conditions, the at least one active device is biased by the adjusting to consume less power, conserving power in the amplifying.

15. A method of low-noise amplification improved for

(i) conserving power during nominal small-signal conditions and also for

(ii) increasing amplification gain, reducing amplification noise figure, and increasing linearity during jamming, making less likely any loss of data,

the method comprising:

amplifying, in at least one active device and in accordance with a bias signal, an input signal received from an external source so as to produce an amplified output signal;

monitoring a power detector the amplified output signal to produce a detected-power signal;

comparing the detected-power signal with the bias signal to produce a difference signal; and

adjusting, in a dynamic bias control circuit responsively to the difference signal, the bias signal of the at least one active device so as to (i) actively move a load line of this at least one active device until (ii) the difference signal becomes zero at which time (iii) such distortion as might otherwise have appeared in the amplified output signal will be minimized;

wherein when the amplified output signal is large because of a presence of a jamming signal then the moved load line of the at least one active device will permit that (i) a larger input resulting from combination of the jamming signal with the input signal will be amplified (ii) without such distortion as would otherwise occur in amplification of these combined signals should the load line have not been moved.

16. A circuit for detecting a peak power of an a.c. signal, the peak power detector circuit comprising:

a resistive voltage divider, located between a voltage source and ground, producing a reference voltage signal;

a diode connecting at its cathode to both the a.c. signal and to the reference voltage signal; and

an envelope detector connected both to the anode of the diode and to the reference voltage;

wherein output of the detector circuit appears across the envelope detector;

wherein when the a.c. signal is zero then the detector circuit output is equal to the reference voltage;

wherein when the a.c. signal is not zero then the detector circuit output is equal to a sum of (i) the reference voltage, and (ii) a voltage of an envelope of the a.c. signal, which voltage of the envelope of the a.c. signal is equivalent to the power of the a.c. signal.